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10/707,241	11/30/2003	Pei-Ying Lin	ALIP0020USA	1240

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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 05/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,241	LIN, PEI-YING	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/30/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are presented for examination in this application (10,707,241) filed on November 30, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. (US 6,180,864), and in view of Lee et al. (US 5,544,351).

As to claim 1, Furuhashi et al. disclose **a method for accessing data of a computer system** [Tone generation Device and Method, and Distribution Medium (title); figures 2-4], **the computer system comprising**:

a first memory [the DRAM, figure 2, 5];

a second memory [the SRAM, figure 2, 7];

an address decoder [the bus arbiter (figure 2, 2) performs the function of an address decoder because it coordinates and controls the input/output connection between a plurality of DSP (figure 2, 20-1~20-4) and a plurality of components comprising a DRAM (figure 2, 5), a SRAM (figure 2, 7), an instruction cache (figure 2, 6), a FIFO (figure 2, 31), a DMAC (figure 2, 4) and a bit converter (figure 2, 10); and determines which DSP is connected to which component at the present instant; note that there is a second bus, the CPU bus (figure 2, 11), connecting a CPU (figure 2, 3) to a instruction cache (figure

2, 6), a SRAM (figure 2, 7), a bit converter (figure 2, 10) and a host interface (figure 2, 1), thus a second address decoder also exists to coordinate and control the input/output connection between the CPU (figure 2, 3) and the instruction cache (figure 2, 6), the SRAM (figure 2, 7), the bit converter (figure 2, 10) and the host interface (figure 2, 1)];

a digital signal processing unit electrically connected to the address decoder [a plurality of DSP (figure 2, 20-1~20-4) are electronically connected, via the main bus (figure 2, 12), to the bus arbiter (figure 2, 2) which performs the function of an address decoder; note that the CPU (figure 2, 3) also qualifies as a digital signal processor because it operates and processes on digital data];

a demultiplexer [the bus arbiter (figure 2, 2) also performs the function of a demultiplexer because it coordinates and controls the input/output connection between a plurality of DSP (figure 2, 20-1~20-4) and a plurality of components comprising a DRAM (figure 2, 5), a SRAM (figure 2, 7), an instruction cache (figure 2, 6), a FIFO (figure 2, 31), a DMAC (figure 2, 4) and a bit converter (figure 2, 10); and determines which DSP is connected to which component at the present instant; note that there is a second bus, the CPU bus (figure 2, 11), connecting a CPU (figure 2, 3) to a instruction cache (figure 2, 6), a SRAM (figure 2, 7), a bit converter (figure 2, 10) and a host interface (figure 2, 1), thus a second demultiplexer also exists to coordinate and control the input/output connection between the CPU (figure 2, 3) and the instruction cache (figure 2, 6), the SRAM (figure 2, 7), the bit converter (figure 2, 10) and the host interface (figure 2, 1)]] **having an input end electrically connected to the digital**

signal processing unit [figure 2 shows that the input end is connected to the digital signal processing unit (figure 2, 20-1~20-4) at the main bus (figure 2, 12); figure 2 also shows the connection between the CPU and the DRAM], **a first output end electrically connected to the second memory** [figure 2 shows that the output end is connected to the SRAM (figure 2, 7, the corresponding second memory) at the main bus (figure 2, 12); figure 2 also shows the connection between the CPU and the SRAM], **and a control end electrically connected to the address decoder** [the bus arbiter (figure 2, 2) performs the function of an address decoder because it coordinates and controls the input/output connection between a plurality of DSP (figure 2, 20-1~20-4) and a plurality of components comprising a DRAM (figure 2, 5), a SRAM (figure 2, 7), an instruction cache (figure 2, 6), a FIFO (figure 2, 31), a DMAC (figure 2, 4) and a bit converter (figure 2, 10); and determines which DSP is connected to which component at the present instant; note that there is a second bus, the CPU bus (figure 2, 11), connecting a CPU (figure 2, 3) to a instruction cache (figure 2, 6), a SRAM (figure 2, 7), a bit converter (figure 2, 10) and a host interface (figure 2, 1), thus a second address decoder also exists to coordinate and control the input/output connection between the CPU (figure 2, 3) and the instruction cache (figure 2, 6), the SRAM (figure 2, 7), the bit converter (figure 2, 10) and the host interface (figure 2, 1)]; **and**

a multiplexer [the bus arbiter (figure 2, 2) also performs the function of a multiplexer because it coordinates and controls the input/output connection between a plurality of DSP (figure 2, 20-1~20-4) and a plurality of components comprising a DRAM (figure 2, 5), a SRAM (figure 2, 7), an instruction cache (figure 2, 6), a FIFO (figure 2, 31), a

DMAC (figure 2, 4) and a bit converter (figure 2, 10); and determines which DSP is connected to which component at the present instant; note that there is a second bus, the CPU bus (figure 2, 11), connecting a CPU (figure 2, 3) to a instruction cache (figure 2, 6), a SRAM (figure 2, 7), a bit converter (figure 2, 10) and a host interface (figure 2, 1), thus a second multiplexer also exists to coordinate and control the input/output connection between the CPU (figure 2, 3) and the instruction cache (figure 2, 6), the SRAM (figure 2, 7), the bit converter (figure 2, 10) and the host interface (figure 2, 1)] **having an output end electrically connected to the digital signal processing unit** [figure 2 shows that the output end is connected to the digital signal processing unit (figure 2, 20-1~20-4) at the main bus (figure 2, 12); figure 2 also shows the connection between the CPU and the CPU bus], **a first input end electrically connected to the second memory** [figure 2 shows that the input end is connected to the SRAM (figure 2, 7, the corresponding second memory) at the main bus (figure 2, 12); figure 2 also shows the connection between the CPU and the SRAM], **and a control end electrically connected to the address decoder** [the bus arbiter (figure 2, 2) performs the function of an address decoder because it coordinates and controls the input/output connection between a plurality of DSP (figure 2, 20-1~20-4) and a plurality of components comprising a DRAM (figure 2, 5), a SRAM (figure 2, 7), an instruction cache (figure 2, 6), a FIFO (figure 2, 31), a DMAC (figure 2, 4) and a bit converter (figure 2, 10); and determines which DSP is connected to which component at the present instant; note that there is a second bus, the CPU bus (figure 2, 11), connecting a CPU (figure 2, 3) to a instruction cache (figure 2, 6), a SRAM (figure 2, 7), a bit

converter (figure 2, 10) and a host interface (figure 2, 1), thus a second address decoder also exists to coordinate and control the input/output connection between the CPU (figure 2, 3) and the instruction cache (figure 2, 6), the SRAM (figure 2, 7), the bit converter (figure 2, 10) and the host interface (figure 2, 1)]; **and**

the method comprising following steps:

(a) providing the digital signal processing unit [a plurality of DSP (figure 2, 20-1~20-4); note that the CPU (figure 2, 3) also qualifies as a digital signal processor because it operates and processes on digital data] **with a cache memory** [instruction cache, figure 2, 6] **electrically connected to the first memory** [figure 2 shows that the cache is electrically connected to the DRAM (the first memory, figure 2, 5) via the main bus (figure 2, 12); figure 2 also shows that the DRAM is connected to the CPU via the main bus and the CPU bus], **the cache memory having an input end electrically connected to a second output end of the demultiplexer** [figure 2 shows that the cache memory having an input end electrically connected to a second output end of the bus arbiter (i.e., the demultiplexer, figure 2, 2) via the main bus (figure 2, 12); note that there is a second bus, the CPU bus (figure 2, 11), connecting a CPU (figure 2, 3) to a instruction cache (figure 2, 6), a SRAM (figure 2, 7), a bit converter (figure 2, 10) and a host interface (figure 2, 1), thus a second demultiplexer also exists to coordinate and control the input/output connection between the CPU (figure 2, 3) and the instruction cache (figure 2, 6), the SRAM (figure 2, 7), the bit converter (figure 2, 10) and the host interface (figure 2, 1)], **an output end electrically connected to a second input end of the multiplexer** [figure 2 shows that the cache memory having

an output end electrically connected to a second output end of the bus arbiter (i.e., the multiplexer, figure 2, 2) via the main bus (figure 2, 12); note that there is a second bus, the CPU bus (figure 2, 11), connecting a CPU (figure 2, 3) to a instruction cache (figure 2, 6), a SRAM (figure 2, 7), a bit converter (figure 2, 10) and a host interface (figure 2, 1), thus a second multiplexer also exists to coordinate and control the input/output connection between the CPU (figure 2, 3) and the instruction cache (figure 2, 6), the SRAM (figure 2, 7), the bit converter (figure 2, 10) and the host interface (figure 2, 1)], **and a tag stored with an address data** [this is the inherent property of a cache memory and the definition of a tag]; **and (b) when the digital signal processing unit generates an address signal** [the main bus (figure 2, 12) includes both address and data signals, and the DSPs provide both address and data signals onto the main bus when communicating with other components connected to the main bus], **(c) controlling the demultiplexer with the address decoder according to the address signal to transfer the address signal either to the cache memory or to the second memory and to enable the digital signal processing unit to receive contents via the multiplexer either from the cache memory or from the second memory** [the functions performed by the bus arbiter (figure 2, 2); the bus arbiter (figure 2, 2) performs the function of an address decoder, a multiplexer and a de multiplexer because it coordinates and controls the input/output connection between a plurality of DSP (figure 2, 20-1~20-4) and a plurality of components comprising a DRAM (figure 2, 5), a SRAM (figure 2, 7), an instruction cache (figure 2, 6), a FIFO (figure 2, 31), a DMAC (figure 2, 4) and a bit converter (figure 2, 10); and determines which DSP is

connected to which component at the present instant], **(d) comparing the address signal with the address data if the address signal is transmitted to the cache memory, and either transmitting contents of the cache memory corresponding to the address signal via the multiplexer to the digital signal processing unit if the address signal matches the address data or updating contents of the cache memory corresponding to the address signal with contents of the first memory corresponding to the address signal** [this is the typical function of a bus arbiter(figure 2, 2); the bus arbiter (figure 2, 2) performs the function of an address decoder, a multiplexer and a de multiplexer because it coordinates and controls the input/output connection between a plurality of DSP (figure 2, 20-1~20-4) and a plurality of components comprising a DRAM (figure 2, 5), a SRAM (figure 2, 7), an instruction cache (figure 2, 6), a FIFO (figure 2, 31), a DMAC (figure 2, 4) and a bit converter (figure 2, 10); and determines which DSP is connected to which component at the present instant], **(e) updating the address data with the address signal and transmitting the updated contents of the cache memory via the multiplexer to the digital signal processing unit** [Instruction cache 6 is a cache memory where any address can be accessed and data can be read and written; of the programs stored in DRAM 5, it stores programs that are frequently accessed from CPU 3 (column 3, lines 50-53); The data that is pitch-converted by DSP 8-2 is either transferred to and stored in pitch-converted data unit 5c of DRAM 5 or, as necessary, is played back by speaker 50 via multiplexer 9 (column 4, lines 44-47)], **and (f) transmitting contents of the second memory corresponding to the address signal via the multiplexer to the**

digital signal processing unit if the address signal is transmitted to the second memory [SRAM 7 can access any address and read and write data simultaneously from both CPU 3 and DMAC 4; for example, it is a dual-port SRAM and is provided as a data cache, and among the data stored in DRAM 5, it stores data that is frequently accessed from CPU 3. SRAM 7 may have a two-bank composition, one being connected to CPU bus 11 and the other to main bus 12 (column 3, lines 43-49); CPU 3 accesses instruction cache 6, loads and executes the program stored therein, and as necessary accesses SRAM 7 and is supplied with the prescribed data. If there is no data that is needed for SRAM 7, CPU 3 makes a request to DMAC 4 and causes execution of a transfer of data by DMA from DRAM 5 to SRAM 7. If there is no program that is needed for instruction cache 6, CPU 3 makes a request to DMAC 4 and causes execution of a program transfer by DMA from DRAM 5 to instruction cache 6 (column 3, lines 33-42)].

Regarding claim 1, Furuhashi et al. teach the use of a bus arbiter which performs the combined functions of an address decoder, a multiplexer and a demultiplexer instead of separate components of an address decoder, a multiplexer and a demultiplexer.

However, it is well known in the art that the bus arbiter (figure 2, 2) performs the combined functions of an address decoder, a multiplexer and a demultiplexer because it coordinates and controls the input/output connection between a plurality of DSP (figure 2, 20-1~20-4) and a plurality of components comprising a DRAM (figure 2, 5), a SRAM (figure 2, 7), an instruction cache (figure 2, 6), a FIFO (figure 2, 31), a DMAC

(figure 2, 4) and a bit converter (figure 2, 10); and determines which DSP is connected to which component at the present instant.

Further, Lee et al. teach in their invention "Digital Signal Processing system Utilizing Relatively Slower Speed Memory" an apparatus comprising a DSP [figure 1,1], a multiplexer [figure 1, 4] and a plurality of demultiplexers [figure 1, 2 and 32] and an address decoder comprising a plurality of address controller signals [CA1~CA5, figure 1, 33~37; column 2, lines 53-56] in a structure conforming to the limitation of "separate components of an address decoder, a multiplexer and a demultiplexer" recited in claim 1.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicant's invention to recognize that the recited limitation of claim 1 of using an address decoder, a multiplexer, and a de multiplexer is a well-known and commonly used structure, either with separate functional elements, as demonstrated by Lee et al., or with a combined functional component such as a bus arbiter, as demonstrated by Furuhashi et al., hence lacking patentable significance.

As to claim 2, Furuhashi et al. teach that **the method of claim 1 wherein the address decoder, the second memory, the digital signal processing unit, the demultiplexer, the multiplexer, and the cache memory are all integrated into a digital signal processing chip** [figure 2 shows that all these components are integrated into a media processor device (figure 2, 60); abstract; further, figure 2 shows that the DSP chip includes a DMAC, program RAM, data RAM, DSP code, audio interface in a signal device]

As to claim 3, Furuhashi et al. teach that **the first memory is a dynamic random access memory (DRAM)** [the DRAM, figure 2, 5].

As to claim 4, Furuhashi et al. teach that **the second memory is a static random access memory (SRAM)** [the SRAM, figure 2, 7].

As to claim 5, refer to "As to claim 1" presented earlier in this Office Action.

As to claim 6, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 7, refer to "As to claim 3" presented earlier in this Office Action.

As to claim 8, refer to "As to claim 4" presented earlier in this Office Action.

4. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Hazelzet et al., (US 6,446,163), "Memory Card with Signal Processing Element."
- kang et al., (US Patent Application Publication 2004/0153524), "Multiprocessor system and Method for operating a Multiprocessor system."
- Dowling, (US Patent Application Publication 2002/0087845), "Embedded-DRAM-DSP Architecture."
- Combs, (US 6,173,358), "Computer system Having Dual Bus Architecture with Audio/Video/CD Drive Controller/Coprocessor Having Integral Bus Arbitrator."

Conclusion

5. Claims 1-8 are rejected as explained above.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

May 1, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
5/18/06